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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/649,218
Filing Date: August 26, 2003
Appellant(s): KIRN, LARRY

John G. Posa
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 6/23/06 appealing from the Office action mailed 10/18/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

The summary of claimed subject matter contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

4,065,765	Wagner	12-1977
3,760,412	Barnes	9-1973

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Wagner.

Wagner discloses a method of demodulating a pulsewidth-modulated data stream (Col. 2, lines 52-55; Col. 6, lines 10-13) using an asynchronous clock (Col.1, lines 63-67, Col.7, line 27-29), comprising the steps of: measuring a temporal aspect of the asynchronous clock (Col.1, lines 65-67; Figures 2 and 3 show timing diagram, for clarity, see column 5, line 30-31 and 53-54: "Recorder 106 provides clock signal C, having a series of 36 pulses" It is noted that the 36 pulses are resulted from measuring the number of pulses) and locking onto the data stream in accordance with the measured periods (Col. 5, lines 57-66: "OR gate 143 the output of which is connected to the clock input C of shift register 139" For clarity, DATA SIGNAL 3 is locking onto (synchronized with) the RECORDER CLOCK SIGNAL C during one complete data cycle, see 36-bit shift register 139: input D, clock input C and Binary DATA OUT).

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Barnes.

Barnes discloses a nonsynchronous binary demodulator which would necessarily perform the method of demodulating a pulsewidth-modulated data stream (10) using an asynchronous clock (14, independent from data input), comprising the step of: measuring a temporal aspect (24 produces f0 or f0/2, see col. 5, lines 53-55) of the asynchronous clock (14 having f0) and locking onto the data stream (10 DATA INPUT) in accordance with the measured periods (output of 24). For clarification, item 24 produces f0 or f0/2, the compensated clock F by measuring the clock signals from 14 in response to the DATA OUT signal 26, (see compensated clock F in Fig. 2) and the data stream (10) is then input to GATES 28 and 30 with the compensated clock F, which means that these GATES are locking onto the data stream 10 in accordance with the compensated clock F.

Regarding claims 2 and 3, the ratio of measured periods is 2:1 (24 produces f0 or f0/2, see also Col. 5, line 37-56)

(10) Response to Argument

Regarding applicant comments directed rejection of claim 1 under U.S.C 102(b) over Wagner, Applicant argues "Nowhere, can Appellant find in Wagner, the teaching of measuring a temporal aspect of the clock and locking onto the data stream in accordance with a measured period. Column 1, line 46 simply states that by means of an index signal, which is synchronized with the input data..., which does not refer to an asynchronous clock. Rather, according to the Wagner disclosure, an index signal is synchronized with the data input which is derived from a rotating light source" For

clarification, "measuring a temporal aspect of the clock" corresponds to the RECORDER CLOCK SIGNAL C having 36-pulses. The 36 pulses are resulted from measuring the clock signal. And "locking onto the data stream in accordance with [a] the measured periods" corresponds to the input to output process using RECORDER CLOCK SIGNAL C in 36-bit SHIFT RESISTER 139 or 141. It is noted that the device of Wagner employs a pair of asynchronous clocking systems, one for controlling data and the other for controlling the recorder (col. 1, 65-68) and "synchronized with the data input" in Col.1, line 46 means that an index signal is synchronized with the data input which controls for locking onto the data stream in accordance with the RECORDER CLOCK SIGNAL C.

Regarding applicant comments directed rejection of claims 1-3 under U.S.C 102(b) over Barnes, Applicant argues "With respect to the step of measuring a temporal aspect of an asynchronous clock, the Examiner simply states that 24 producing f0 or f0/2 of an asynchronous clock [(10)] (14) having a frequency of f0. Be that as it may, this is not used to lock onto a data stream." For clarification, as mentioned above, item 24 produces f0 or f0/2, the compensated clock F by measuring the clock signals from 14 in response to the DATA OUT signal 26, (see compensated clock F in Fig. 2) and the data stream (10) is then input to GATES 28 and 30 with the compensated clock F, which means that these GATES are locking onto the data stream 10 in accordance with the compensated clock F. It is noted that since the term "lock" is not defined or disclosed in the specification, the term "lock" is interpreted in an ordinary term used in the art. When two or more input conditions are met through a device such as a comparator or a

conditioning logic gate, one of the inputs are considered "locked" in accordance with other input. In this case, the logic gates 28 and 30 lock the data stream in accordance with the compensated clock F.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Joseph Chang

9/12/06

Conferees:

Robert J. Pascal

David S. Blum